AMENDMENTS TO THE CLAIMS

1.(currently amended): A turbo decoder for iteratively decoding received signals up to a set number of times comprising:

first and second elementary decoders for executing first decoding processing using a received signal, then executing second decoding processing using interleaved results of the first decoding processing and also using another received signal, and subsequently executing repeatedly, first decoding processing using deinterleaved results of the second decoding processing and also using said received signal and second decoding processing using interleaved results of the first decoding processing and also using said other received signal;

an error detector for detecting errors in results of the first decoding processing in parallel with a decoding operation of the second decoding processing; and

a controller which, when absence of error has been detected in results of the first decoding processing, is operable for outputting the results of the first decoding processing and halting the decoding operation of the second decoding processing even if the number of times decoding has been performed has not attained said set number of times.

2.(currently amended): A turbo decoder for iteratively decoding [[a]] received [[signal]] signals up to a set number of times comprising:

first and second elementary decoders for executing first decoding processing using a received signal, then executing second decoding processing using interleaved results of the first decoding processing and also using another received signal, and subsequently executing repeatedly, first decoding processing using deinterleaved results of the second decoding

processing and also using said received signal and second decoding processing using interleaved results of the first decoding processing and also using said other received signal;

an error detector for detecting errors in results of decoding in parallel with a decoding operation; and

a controller which, when absence of error has been detected, is operable for outputting results of decoding and halting the decoding operation even if the number of times decoding has been performed ~~has not attained said~~ is not a set number of times,

wherein said controller monitors the number of times errors are detected in decoded results [[when]] after decoding has been performed said set number of times and executes the decoding operation further if the number of times errors are detected is equal to or less than a set value.

3.(cancelled)

4.(currently amended): A turbo decoder for receiving first data ya, second data yb obtained by encoding said first data, and third data yc obtained by interleaving and then encoding said first data, and executing decoding processing repeatedly using these received signals, comprising:

first and second elementary decoders for executing first decoding processing using interleaved result of received signal [[signals]] ya and also using received signal yc, then executing second decoding processing using deinterleaved results of the first decoding processing and also using received signal yb, and subsequently executing, repeatedly, first decoding processing using interleaved results of the second decoding processing and also using

said received signal yc, and second decoding processing using deinterleaved results of the first decoding processing and also using said received signal yb;

an interleaving unit for interleaving the received signal ya and the results of the second decoding processing and inputting the same to the first elementary decoder; and

a deinterleaving unit for deinterleaving the results of the first decoding processing and inputting the same to the second elementary decoder;

wherein in order to render an error pattern in decoded bursty data, results of final decoding processing are output from said second elementary decoder directly without intervention of interleaving or deinterleaving.

5.(currently amended): A turbo decoder for receiving first data ya, second data yb obtained by encoding said first data, and third data yc obtained by interleaving and then encoding said first data, and executing decoding processing repeatedly using these received signals, comprising:

one elementary decoder for executing first decoding processing using an interleaved result of received signal [[signals]] ya and also using received signal yc, then executing second decoding processing using deinterleaved results of the first decoding processing and also using received signal yb, and subsequently executing, repeatedly, first decoding processing using interleaved results of the second decoding processing and also using said received signal yc; and second decoding processing using deinterleaved results of the first decoding processing and also using said received signal yb;

an interleaving unit for interleaving the received signal ya and inputting the same to the elementary decoder;

a selection circuit for selecting the signal yc when the first decoding processing is executed, selecting the signal yb when the second decoding processing is executed, and inputting the selected signal to the elementary decoder; and

means for deinterleaving results of the first decoding processing, interleaving results of the second decoding processing and inputting the deinterleaved and interleaved results to the elementary decoder; wherein results of decoding are output from said elementary decoder directly without intervention of interleaving or deinterleaving.

6.(currently amended): A turbo decoder for iteratively decoding [[a]] received [[signal]] signals up to a set number of times, comprising:

first and second elementary decoders for executing [[second]] first decoding processing using a received signal, then executing second decoding processing using interleaved results of [[applying]] the first decoding processing ~~to a prescribed received signal,~~ and also using another received signal, and subsequently executing, repeatedly, first decoding processing using deinterleaved results of the second decoding processing and also using said [[prescribed]] received signal, and second decoding processing using interleaved results of first decoding processing and also using said other received signal; [[and]]

an interleaving unit for interleaving the results of the first decoding processing and inputting the same to the second elementary decoder;

a deinterleaving unit for deinterleaving the results of the second decoding processing and inputting the same to the first elementary decoder; and

a selection circuit for selecting and outputting the results of first and second decoding processing output from said first and second elementary decoders based upon which of a bursty error pattern and a random error pattern is requested in decoded data;

wherein the nature of an error generation pattern in decoded data finally output is controlled by selecting the decoded data to be output.

7.(currently amended): A turbo decoder for iteratively decoding [[a]] received [[signal]] signals up to a set number of times comprising:

first and second elementary decoders for executing [[second]] first decoding processing using ~~results of applying first decoding processing to a first received signal, and also using another received signal, and subsequently executing, repeatedly, first decoding processing using results of second decoding processing and also using said first received signal, and second decoding processing using results of first decoding processing and also using said other received signal; and~~ a received signal, then executing second decoding processing using interleaved or deinterleaved results of the first decoding processing and also using another received signal, and subsequently executing repeatedly, first decoding processing using deinterleaved or interleaved results of the second decoding processing and also using said received signal and second decoding processing using interleaved or deinterleaved results of the first decoding processing and also using said other received signal;

a first interleaving unit and a first deinterleaving unit for respectively interleaving and deinterleaving the results of the first decoding processing and inputting the same to the second elementary decoder;

a second deinterleaving unit and a second interleaving unit for respectively deinterleaving and interleaving the results of the second decoding processing and inputting the same to the first elementary decoder;

a first selection circuit for selecting a combination of received signals[[,]] input to the first elementary decoder that executes said first decoding processing and selecting a received signal input to the second elementary decoder that executes the second decoding processing based upon which of a bursty error pattern and a random error pattern is requested in decoded data;

a second selection circuit for selecting the interleaved results of the first interleaving unit and the deinterleaved results of the first deinterleaving unit and inputting the same to the second elementary decoder based upon which of a bursty error pattern and a random error pattern is requested in decoded data; and

a third selection circuit for selecting the deinterleaved results of the second deinterleaved unit and the interleaved results of the second interleaving unit and inputting the same to the second elementary decoder based upon which of a bursty error pattern and a random error pattern is requested in decoded data;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals and switching the interleaved results and the deinterleaved results input to the first and second elementary decoders.

8.(currently amended): A turbo decoder for receiving first data ya, second data yb obtained by encoding said first data, and third data yc obtained by interleaving and then

encoding said first data, and executing decoding processing repeatedly using these received signals, ~~iteratively decoding a received signal a set number of times~~ comprising:

[[one]] an elementary decoder for executing [[second]] first decoding processing using interleaved results of ~~applying first decoding processing to a~~ received signal yc, then executing second decoding processing using deinterleaved results of the first ~~and also using another received signal, and subsequently executing, repeatedly, first decoding processing using results of second~~ decoding processing and also using said received signal yb, and subsequently executing repeatedly, first decoding processing using interleaved results of the second decoding processing and also using said received signal yc; and second decoding processing using deinterleaved results of the first decoding processing and also using said [[other]] received signal yb; and

an interleaving unit for interleaving the received signal ya and inputting the same to the first elementary decoder;

an interleaving unit and a deinterleaving unit for respectively interleaving and deinterleaving the results of the second and first decoding processing and inputting the same to the elementary decoder;

a first selection circuit for selecting a combination of received signals input to the elementary decoder at a timing at which said first decoding processing is executed, and selecting a received signal input to the elementary decoder at a timing at which said second decoding processing is executed; and

a second selection circuit for selecting the interleaved results of the interleaving unit and the deinterleaved results of the deinterleaving unit at timings of said second and first decoding processing and inputting the same to the elementary decoder;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals and switching the interleaved results and the deinterleaved results input to the elementary decoder at the timings of the first and second decoding processing.

9.(cancelled)

10.(currently amended): A turbo decoder ~~for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, executing second decoding processing using a second set of signals including a second received signal selected from among the received signals and subsequently executing repeatedly, first and second decoding processing, comprising:~~ according to claim 1, wherein said

[[an]] error detector ~~for detecting~~ detects errors in results of the first decoding processing while the second decoding processing is being executed.

11.(currently amended): A turbo decoder ~~for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, executing second decoding processing using the results of the first decoding processing and a second set of signals including a second received signal selected from among the received signals and subsequently executing repeatedly, first and second decoding processing, comprising:~~ according to claim 1, further comprising:

a memory for storing the results of the first decoding processing; and

~~an error detector for detecting errors in the results of the first decoding processing; and~~

means for outputting the results of the first decoding processing stored in said memory in accordance with the result of the error detection.

12.(currently amended): The turbo decoder according to claim [[11]] 1, wherein said memory stores the results of the first and second decoding processing alternately.

13.(currently amended): The turbo decoder according to claim [[11]] 1, wherein a signal obtained by interleaving the results of the first decoding processing is used for the second decoding processing.

14-24.(cancelled)